ModelSim®

Comparison of ModelSim PE, LE, and SE Products

FEATURE	ModelSim PE	ModelSim LE	ModelSim SE
GENERAL			
Licensing - Floating License	OPTION	OPTION	■
Language Neutral License			OPTION
ASIC Sign-Off			■
IP Support	■	■	■
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates & Wizards	■	■	■
Platform-Independent Compiled Database	■	■	■
Native-Compile Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatibility			■
LANGUAGES			
VHDL	■		■
Verilog	■	■	■
Mixed Language	OPTION		OPTION
SystemC		OPTION	OPTION
Verilog 2001	■	■	■
SystemVerilog - Phase 1 (No Testbenches or Assertions)	■	■	■
Analog/Mixed-Signal			OPTION (Advance MS Product)
Verilog PLI/VPI	■	■	■
VHDL FLI			■
DEBUG			
Source Code Debugging	■	■	■
Dataflow Window	OPTION	■	■
C Debugger		OPTION (with SystemC)	■
Memory Window	■	■	■
Extra Standalone Viewers	OPTION	OPTION	OPTION
Multiple Waveform Windows			■
Code Coverage	OPTION	OPTION	■
Toggle Coverage	OPTION	OPTION	■
ChaseX Feature	OPTION	■	■
Waveform Compare	OPTION	■	■
Signal Spy	■	■	■
User-Customizable GUI (via Tk)			■
SIMULATION			
Single-Kernel Simulation Engine	■	■	■
Verilog Global Optimization			■
Verilog Gate Acceleration			■
Performance Analyzer			■
Separate Elaborate Option			■
Waveform Management Toolset	■	■	■
VCD & Extended VCD Support	■	■	■
VCD Re-simulation			■
Batch Mode Simulation	■	■	■
Interactive Simulation	■	■	■
Checkpoint & Restore			■
SWIFT Interface / SmartModels	OPTION	OPTION	■
Synopsys Hardware Modeler Support			■
PLATFORM SUPPORT			
32-Bit OS Support	WINDOWS 98/NT/ME/2000/XP	LINUX	AIX, HP-UX, LINUX + SOLARIS, WINDOWS 98/NT/ME/2000/XP
64-Bit OS Support			AIX, LINUX (ITANIUM-2), HP-UX, SOLARIS
Intel Itanium-2 Support			HP-UX, LINUX